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EXAMINER	
CHU, GABRIEL L	
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SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/763,009	Applicant(s) HOUSTY, OSWIN	
	Examiner Gabriel L. Chu	Art Unit 2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,8-10,12-14,16-19 and 22-25* is/are rejected.

7)☒ Claim(s) *4,7,11,15,20,21,26 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. **Claim 9, 10, 12, 14 rejected under 35 U.S.C. 102(b) as being anticipated by US 5327548 to Hardell, Jr. et al.** See previous office action.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1-3, 5, 6, 8 rejected under 35 U.S.C. 103(a) as being unpatentable over US 5327548 to Hardell, Jr. et al. in view of US 5740349 to Hasbun et al. and US 5867702 to Lee.**

5. Referring to claim 1, Hardell discloses in a multiprocessor computer system having a plurality of processing nodes coupled to an array wherein each processing node is coupled to at least one other processing node, and a memory distributed among the plurality of processing nodes (see figure 1), a method of testing the memory comprising the steps of:

determining a configuration of the array (See figure 1, where a configuration of

processors has been determined. Further, a single boot processor is selected, coordinating action between the multiple processors, abstract.);

testing the memory over the array to identify a bad memory element; and forming a revised configuration that excludes said bad memory element (From line 66 of column 1, "The present invention defines a system and method for steering spare bits in a multi-processor architecture having global memory resources, being comprised of a means for selecting a first processor to define the steering of spare bits in global memory, a means for enabling processors to define the steering of spare bits in respective local memories, and means for transferring global memory spare bit steering information from the first processor to other processors. In a preferred practice of the invention, the first of the multi-processors reaching a specified stage in the booting process is assigned responsibility for testing both its local memory and the global memory. The remaining processors test only their respective local memory arrays. The bit steering information derived by the selected processor is thereafter conveyed to each of the other processors as a part of ensuring that the memory spare bit steering is consistent from processor to processor for the global memory. Local memory bit steering is individualized to the associated processor.").

Although Hardell does not specifically disclose determining an initial configuration of the memory, testing according to said initial configuration, and modifying said initial configuration to form the revised configuration, testing memory using an "initial configuration" that is subsequently modified is known in the art. An example of this is shown by Hasbun, from figure 7, it can be seen that at powerup, a bad block table is

read from flash ROM into RAM and subsequently detected bad blocks are written to the block table in RAM. A person of ordinary skill in the art at the time of the invention would have been motivated to use a bad block table read from flash ROM because, from line 29 of column 3 of Hasbun, "provide a method by which defects in the flash memory array may be reliably stored for the management of blocks of flash EEPROM memory" and from line 39 of column 3 of Hasbun, "writes those changes to read only memory apart from the array so that they are available to the controller should power be lost during the operation of the array." As can be seen from figure 1 of Hardell, configuration registers are used to store mapping information, such registers not being disclosed as non-volatile, and as such, prone to unreliability as disclosed in Hasbun.

Further, although Hardell does not specifically disclose each processing node is directly coupled to at least one other processing node, this is known in the art. The scope of the term "directly" is read in light of Applicant's specification paragraph 23, although no limitations are read into the claim. An example of this is shown by Lee, from line 57 of column 2, "The processors communicate with each other and with system memory 140 across a high speed system bus 150." A person of ordinary skill in the art at the time of the invention would have been motivated to directly couple processing nodes because, as disclosed by Lee, it allows "the processors [to] communicate with each other", as further motivated from line 19 of column 1, "More recently, interest in multiple processor systems has increased as a consequence of the low cost and high performance of microprocessors, with the objective of replicating mainframe performance through the parallel use of multiple microprocessors." Further, Hardell

discloses, from line 23 of column 1, "Systems composed of multiple but coordinated processors were first developed and used in the context of mainframes. More recently, interest in multiple processor systems has escalated as a consequence of the low cost and high performance of microprocessors, with the objective of replicating mainframe performance through the parallel use of multiple microprocessors."

6. Referring to claim 2, Hardell in view of Hasbun and Lee discloses passing control of the multiprocessor computer system with said revised configuration to an operating system (From line 56 of column 2 of Hardell, "Included within the system are four processors, identified by reference numerals 1-4. A representative example of a processor is the RISC System/6000 workstation with associated AIX Operating System as is commercially available from IBM Corporation." From figure 3, "continue system boot".).

7. Referring to claim 3, Hardell in view of Hasbun and Lee discloses said step of modifying said initial configuration to form said revised configuration comprises the steps of: identifying a bad memory block corresponding to said bad memory element; forming said revised configuration to exclude said bad memory block (From line 66 of column 1 of Hardell, "The present invention defines a system and method for steering spare bits in a multi-processor architecture having global memory resources, being comprised of a means for selecting a first processor to define the steering of spare bits in global memory, a means for enabling processors to define the steering of spare bits in respective local memories, and means for transferring global memory spare bit steering information from the first processor to other processors. In a preferred practice

of the invention, the first of the multi-processors reaching a specified stage in the booting process is assigned responsibility for testing both its local memory and the global memory. The remaining processors test only their respective local memory arrays. The bit steering information derived by the selected processor is thereafter conveyed to each of the other processors as a part of ensuring that the memory spare bit steering is consistent from processor to processor for the global memory. Local memory bit steering is individualized to the associated processor.").

8. Referring to claim 5, Hardell in view of Hasbun and Lee discloses identifying one of the plurality of processing nodes that is to be a boot strap processor; performing said step of testing using said boot strap processor (See Hardell figure 3, "test global memory" performed by processor 0.).

9. Referring to claim 6, Hardell in view of Hasbun and Lee discloses said step of modifying said initial configuration to form said revised configuration comprises the step of: communicating said revised configuration to each of the plurality of processing nodes (See figure 3 of Hardell, "send bit steering and bank configuration to other processors via atomic complex and/or global memory".).

10. Referring to claim 8, Hardell in view of Hasbun and Lee discloses said step of determining said initial configuration comprises the step of determining said initial configuration using a system management bus coupled to the memory (Hasbun, from figure 7, shows that at powerup, a bad block table is read from flash ROM into RAM and subsequently detected bad blocks are written to the block table in RAM. Such data transfer for system management is accomplished using a bus.).

11. **Claim 13 rejected under 35 U.S.C. 103(a) as being unpatentable over US 5327548 to Hardell, Jr. et al. as applied to claim 12 above, and further in view of US 5740349 to Hasbun et al.** See previous office action

12. **Claims 16-19 rejected under 35 U.S.C. 103(a) as being unpatentable over US 5327548 to Hardell, Jr. et al. in view of US 5740349 to Hasbun et al. and US 6571347 to Tseng and US 5867702 to Lee.** Referring to claim 16, Hardell discloses for use in a multiprocessor computer system including: a plurality of processing nodes coupled in an array wherein each processing node is coupled to at least one other processing node; and a memory distributed among the plurality of nodes (see figure 1),

a boot coordinating means adapted to be coupled to one of the plurality of processing nodes designated a boot strap processor (BSP) (From the abstract, "During the system boot cycle one of the multiple processors is selected to test global memory and to configure the steering of the spare bits by bank or the like."), , said boot coordinating means comprising:

a first set of instructions executable by said BSP to determine a configuration of the array (See figure 1, where a configuration of processors has been determined. Further, a single boot processor is selected, coordinating action between the multiple processors, abstract.);

a third set of instructions executable by said BSP to test the memory over the array to identify a bad memory element; and a fourth set of instructions executable by said BSP to form a revised configuration that excludes said bad memory element (From line 66 of column 1, "The present invention defines a system and method for steering

spare bits in a multi-processor architecture having global memory resources, being comprised of a means for selecting a first processor to define the steering of spare bits in global memory, a means for enabling processors to define the steering of spare bits in respective local memories, and means for transferring global memory spare bit steering information from the first processor to other processors. In a preferred practice of the invention, the first of the multi-processors reaching a specified stage in the booting process is assigned responsibility for testing both its local memory and the global memory. The remaining processors test only their respective local memory arrays. The bit steering information derived by the selected processor is thereafter conveyed to each of the other processors as a part of ensuring that the memory spare bit steering is consistent from processor to processor for the global memory. Local memory bit steering is individualized to the associated processor.").

Although Hardell does not specifically disclose a second set of instructions executable by the BSP to determine an initial configuration of the memory, testing according to said initial configuration, and modifying said initial configuration to form the revised configuration, testing memory using an "initial configuration" that is subsequently modified is known in the art. An example of this is shown by Hasbun, from figure 7, it can be seen that at powerup, a bad block table is read from flash ROM into RAM and subsequently detected bad blocks are written to the block table in RAM. A person of ordinary skill in the art at the time of the invention would have been motivated to use a bad block table read from flash ROM because, from line 29 of column 3 of Hasbun, "provide a method by which defects in the flash memory array may be reliably

stored for the management of blocks of flash EEPROM memory" and from line 39 of column 3 of Hasbun, "writes those changes to read only memory apart from the array so that they are available to the controller should power be lost during the operation of the array." As can be seen from figure 1 of Hardell, configuration registers are used to store mapping information, such registers not being disclosed as non-volatile, and as such, prone to unreliability as disclosed in Hasbun.

Further, although Hardell does not specifically disclose each processing node is directly coupled to at least one other processing node, this is known in the art. The scope of the term "directly" is read in light of Applicant's specification paragraph 23, although no limitations are read into the claim. An example of this is shown by Lee, from line 57 of column 2, "The processors communicate with each other and with system memory 140 across a high speed system bus 150." A person of ordinary skill in the art at the time of the invention would have been motivated to directly couple processing nodes because, as disclosed by Lee, it allows "the processors [to] communicate with each other", as further motivated from line 19 of column 1, "More recently, interest in multiple processor systems has increased as a consequence of the low cost and high performance of microprocessors, with the objective of replicating mainframe performance through the parallel use of multiple microprocessors." Further, Hardell discloses, from line 23 of column 1, "Systems composed of multiple but coordinated processors were first developed and used in the context of mainframes. More recently, interest in multiple processor systems has escalated as a consequence of the low cost and high performance of microprocessors, with the objective of replicating mainframe

performance through the parallel use of multiple microprocessors."

Further, although Hardell does not specifically disclose that the boot coordination means may be a BIOS, using a BIOS for booting a system is well known in the art. An example of this is shown by Tseng, From line 1 of column 4, "Flash memory 12 contains a computer initiation program, or BIOS program, used to boot-up host system 40 to which apparatus 10 is connected." A person of ordinary skill in the art at the time of the invention would have been motivated to use a BIOS because Hardell has specifically disclosed a need for computer initiation which the BIOS fulfills. Further, Lee has disclosed a particularly BIOS-like component, from line 25 of column 2, "In the preferred embodiment, a single copy of the boot code is stored in a global read-only memory (ROM) for utilization by each of the multiple processors.", such component responsible for boot testing, e.g., the paragraph beginning line 37 of column 3.

13. Referring to claim 17, Hardell in view of Hasbun, Lee, and Tseng discloses said first, second, third, and fourth sets of instructions are stored in a mask ROM (From line 3 of column 4 of Tseng, "Because the BIOS program is stored in flash memory, the program may be edited, altered, or over-written. ROM 14 stores the same BIOS program as does flash memory 12 before the program stored in flash memory 12 is altered in any manner. ROM 14 may be a Mask ROM, OTP ROM, EPROM, EEPROM, and a flash memory.").

14. Referring to claim 18, Hardell in view of Hasbun, Lee, and Tseng discloses said first, second, third, and fourth sets of instructions are stored in an EPROM (From line 3 of column 4 of Tseng, "Because the BIOS program is stored in flash memory, the

program may be edited, altered, or over-written. ROM 14 stores the same BIOS program as does flash memory 12 before the program stored in flash memory 12 is altered in any manner. ROM 14 may be a Mask ROM, OTP ROM, EPROM, EEPROM, and a flash memory.").

15. Referring to claim 19, Hardell in view of Hasbun, Lee, and Tseng discloses passing control of the multiprocessor computer system with said revised configuration to an operating system (From line 56 of column 2 of Hardell, "Included within the system are four processors, identified by reference numerals 1-4. A representative example of a processor is the RISC System/6000 workstation with associated AIX Operating System as is commercially available from IBM Corporation." From figure 3, "continue system boot".).

16. **Claims 22-25 rejected under 35 U.S.C. 103(a) as being unpatentable over US 5327548 to Hardell, Jr. et al. in view of US 6571347 to Tseng.** Referring to claim 22, Hardell discloses for use in a multiprocessor computer system including a plurality of processing nodes coupled in an array wherein each processing node is coupled to at least one other processing node; and a memory distributed among the plurality of processing nodes (see figure 1),

a boot coordination means adapted to be coupled to one of the plurality of processing nodes, designated a boot strap processor (BSP) (From the abstract, "During the system boot cycle one of the multiple processors is selected to test global memory and to configure the steering of the spare bits by bank or the like."), said boot coordination means comprising:

a first set of instructions executable by said BSP to configure the memory by programming the plurality of processing nodes with an initial configuration (From line 33 of column 4, "Since the first processor to reach a certain stage in the booting process assumes the responsibilities of processor 0, the parallel character always remains intact." From line 21 of column 4, "It is presumed that processor 0 acquires responsibility for testing global memory.");

a second set of instructions executable by said BSP to test the memory using said initial configuration to identify a bad memory element (From line 21 of column 4, "It is presumed that processor 0 acquires responsibility for testing global memory.");

a third set of instructions executable by said BSP to determine a node and a region defined on said node which are associated with said bad memory element; a fourth set of instructions executable by said BSP to reconfigure the memory by programming the plurality of processing nodes with a revised configuration that excludes said region (From line 66 of column 1, "The present invention defines a system and method for steering spare bits in a multi-processor architecture having global memory resources, being comprised of a means for selecting a first processor to define the steering of spare bits in global memory, a means for enabling processors to define the steering of spare bits in respective local memories, and means for transferring global memory spare bit steering information from the first processor to other processors. In a preferred practice of the invention, the first of the multi-processors reaching a specified stage in the booting process is assigned responsibility for testing both its local memory and the global memory. The remaining processors test

only their respective local memory arrays. The bit steering information derived by the selected processor is thereafter conveyed to each of the other processors as a part of ensuring that the memory spare bit steering is consistent from processor to processor for the global memory. Local memory bit steering is individualized to the associated processor." Further, see figure 1.); and

a fifth set of instructions executable by said BSP to operate the multiprocessor computer system using said revised configuration (From line 56 of column 2 of Hardell, "Included within the system are four processors, identified by reference numerals 1-4. A representative example of a processor is the RISC System/6000 workstation with associated AIX Operating System as is commercially available from IBM Corporation." From figure 3, "continue system boot".).

Although Hardell does not specifically disclose that the boot coordination means may be a BIOS, using a BIOS for booting a system is well known in the art. An example of this is shown by Tseng, From line 1 of column 4, "Flash memory 12 contains a computer initiation program, or BIOS program, used to boot-up host system 40 to which apparatus 10 is connected." A person of ordinary skill in the art at the time of the invention would have been motivated to use a BIOS because Hardell has specifically disclosed a need for computer initiation which the BIOS fulfills.

17. Referring to claim 23, Hardell in view of Tseng discloses said first, second, third, fourth, and fifth sets of instructions are stored in a mask ROM (From line 3 of column 4 of Tseng, "Because the BIOS program is stored in flash memory, the program may be edited, altered, or over-written. ROM 14 stores the same BIOS program as does flash

memory 12 before the program stored in flash memory 12 is altered in any manner. ROM 14 may be a Mask ROM, OTP ROM, EPROM, EEPROM, and a flash memory.").

18. Referring to claim 24, Hardell in view of Tseng discloses said first, second, third, fourth, and fifth sets of instructions are stored in an EPROM (From line 3 of column 4 of Tseng, "Because the BIOS program is stored in flash memory, the program may be edited, altered, or over-written. ROM 14 stores the same BIOS program as does flash memory 12 before the program stored in flash memory 12 is altered in any manner. ROM 14 may be a Mask ROM, OTP ROM, EPROM, EEPROM, and a flash memory.").

19. Referring to claim 25, Hardell in view of Tseng discloses said fifth set of instructions operates the multiprocessing computer system using said revised configuration by transferring control to an operating system (From line 56 of column 2 of Hardell, "Included within the system are four processors, identified by reference numerals 1-4. A representative example of a processor is the RISC System/6000 workstation with associated AIX Operating System as is commercially available from IBM Corporation." From figure 3, "continue system boot".).

Allowable Subject Matter

20. **Claim 4, 7, 11, 15, 20, 21, 26, 27 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.** See previous office action.

Response to Arguments

21. Applicant's arguments filed 6 November 2006 have been fully considered but they are not persuasive.

22. Applicant argues on page 10 that neither Hardell nor Hasbun "determines a configuration of an array of processing nodes" and page 11, neither Hardell, Hasbun, or Tseng has "a set of instructions that determines a configuration of an array of processing nodes", further relying upon Applicant's specification for an example of how configuration of processing nodes may be determined (figure 2, paragraph 38). Firstly, Examiner notes the breadth of "determining a configuration of the array", as in claim 1. Broadly and reasonably, this may merely mean that some configuration of the array of processing nodes is determined. Note that there is no mention of what this configuration is, how it is determined, when it is determined, or even what is done with this determination.

Secondly, even in view of the more specific limitation of claim 16 that states that it must be a first set of instructions executable by said BSP to determine this configuration, Hardell meets the limitations. For example, from the abstract of Hardell, "During the system boot cycle one of the multiple processors is selected to test global memory and to configure the steering of the spare bits by bank or the like." This is a boot coordination means (which in view of Tseng, may be BIOS), which acts in conjunction with a selected processor to act as the boot service processor. This Hardell BSP then may perform a broadly interpretable action that meets Applicant's claimed "determine a configuration of the array". For example, that this selected processor now

executes the global memory test "determines" the test processor "configuration" of the array. Further, in figure 3, the processor set to test global memory, processor 0, then "determines" the "configuration" of the global memory, an aspect of the array, and sends this information to the other processors. Further, that this Hardell BSP sends this configuration information itself indicates that the Hardell BSP has determined a configuration of the array so that the memory configuration may be sent to the other processors.

Thirdly, that Applicant must rely on Applicant's specification to support the arguments, rather than the actual claimed invention, is usually a strong indicator that the claims are much broader than Applicant believes. Examiner advises amending to include what Applicants believe to be the invention, or at least the distinction over the applied art.

23. Referring to Applicant's argument (page 10) that Hasbun is not directed to a multiprocessor system, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In this instance, Examiner uses Hasbun to show that it is known in the art to revise an initial configuration subsequent to test.

24. Referring to Applicant's argument (page 11) that Hardell does not configure the plurality of processing nodes with an initial configuration, by citing those particular

passages, Examiner has indicated that the "initial configuration" referred to is mapped to the initial configuration of the processing nodes of Hardell. That this is not what Applicant intends this to be mapped to is an indicator that the claims are much broader than Applicant believes. Examiner advises amending to include what Applicants believe to be the invention, or at least the distinction over the applied art. Further, while Applicant has claimed a "revised configuration", there is no indication what this is a revision from. As applied herein, in view of Hardell, this is revised over whatever configuration Hardell's test processor is using.

It is not until claim 13 that Examiner interprets this to be an initial configuration of the memory. However, this is obviated in view of Hasbun, and Hardell in view of Hasbun teaches that an initial configuration of memory may be transferred for processing and remapping.

25. Referring to Applicant's argument (page 11) that the rejection of claim 9 is "inconsistent" with the position taken with respect to claim 21, Examiner notes that claim 21 is in a wholly different set of claims than claim 9. For example, claim 9 merely claims "an initial configuration". In view of the fact that this is used for programming the processing nodes, this may very well be the configuration of the processing nodes. Claim 21, on the other hand, depends from claim 16, where "an initial configuration of the memory" is contrasted with "a configuration of the array". Examiner puts forth that the position taken is not inconsistent, but merely reflects the inconsistency of Applicant's claim language.

Conclusion

26. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (571) 272-3656. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Gabriel L. Chu
Examiner
Art Unit 2114

gc